

PAN502x
Capacitive Touch Controller Datasheet

PAN502x-A-A, Rev 1.0

PANCHIP

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1. General Description

The PAN502x serial mutual capacitive touch control IC is designed for providing a high reliability and low power consumption touch panel control system with rapidly report rate, pinpoint touch accuracy. It supports up to 10 touch point, large numbers of touch gestures and strong robust to noises which may come from charger, display, RF and so on. PAN502x includes PAN5020 and PAN5021. The main differences between them are that the previous one provides 21TX+ 12RX, supports I2C and SPI interfaces and is packaged with 48Pin QFN, and the later one provides 20TX+11RX , only supports I2C and is packaged with 40Pin QFN.

It can be used in multi-filed. Such as Smart phones, Personal Navigation Devices (PND), Portable Media Players, Mobile Internet Devices (MID) and so forth. The basic features of PAN5020 will be shown in this datasheet in detail.

1.1. Features

- Mutual Capacitive Sensing Techniques
- True Multi-touch with up to 10 Points of Absolute X and Y Coordinates
- Noise Suppression Technologies
 - On-chip 3.3V TX Supply for Higher Signal-to-Noise Ratio(SNR)
 - Immune to RF Interferences
 - Charger Noise Immunity
 - Display Noise Immunity
- Automatic Baseline Tracking to the changing environment
- PAN5020 Supports up to 21 TX lines + 12 RX lines
- PAN5021 Supports up to 20 TX lines + 11 RX lines
- Full Programmable Scan Sequences to Support Various TX/RX Configurations
- High Report Rate: More than 150Hz
- Operating Temperature Range: -20°C to +85°C
- Power (configuration dependent)
 - 2.8V to 3.6V Operating Voltage
 - IO_VCC Connected to External or Internal 1.8V to 3.6V
 - 15mA Average Power Consumption @10 Finger, 150Hz Report Rate
 - 35uA Typical Shutdown Power
- Optimal Sensing Mutual Capacitor: 1pF~4pF
- Host Interfaces :I2C/SPI
 - I2C Slave Mode at Standard Mode and Fast Mode
Bit Rates: 100 kbps, 400 kbps
 - SPI Slave Mode at Bit Rates up to 10 Mbps
- Built-in Enhanced MCU, 12-Bit ADC Accuracy and DSP
- 3 Operating Modes
 - Run
 - Monitor
 - Shutdown

1.2. Applications

- Smart phones
- Personal Navigation Devices (PND)
- Portable Media Players
- Mobile Internet Devices (MID)

2. Functional Block

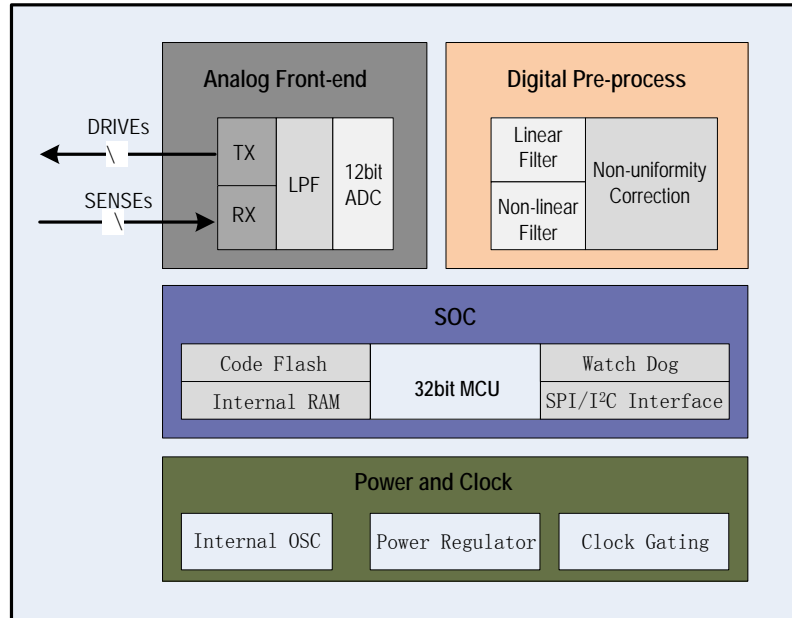


Figure 2-1 PAN502x Functional Block

2.1. Overview

- Touch Panel Interface Circuits

The main function of Analog Front-End (AFE) and its controller is to communicate PAN502x with the touch panel. The drive signal is transmitted to panel by TX and sensed from panel by RX, and then processed by AFE. This process can be configured by FW, and is detailed in the following sections.

- Enhanced 32bit MCU with DSP accelerator

PAN502x contains a high-performance low-power 32-bit MCU with a DSP accelerator. The DSP accelerates the data processing, and reports the processed data to MCU with high rate and low power consumption. The MCU regulates all the Drive signals transmitting, sensing, data processing, reporting and other procedures. It is also optimized for low power and fast response rate.

- External Interface

- I²C/SPI: interfaces for data exchange with host
- INT: an interrupt signal to inform the host that touch data is ready
- nRST: an external low active reset and shunt down the chip.

- A watch dog timer is implemented to ensure the robustness of the chip.

- A voltage regulator to generate 1.8V for internal circuits from the input VDD3 supply.

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2.2. Operation Modes

PAN502x can operate in the following three modes:

- Run Mode

When in this mode, PAN502x actively scans the panel on full speed. The default scan rate is 150 frames per second and it can be configured by host to speed up or slow down.

- Monitor Mode

When in this mode, PAN502x scans the panel at a reduced rate to save power. The default scan rate is 30 frames per second and is regulated by host at real time. In this mode, only a small part of modules operates to determine whether there is a touch or not. Once a touch is detected, PAN502x will enter into the Run mode immediately and calculate and report the touch position. The serial interface is closed and no data will be reported to host in Monitor mode.

- Shutdown Mode

When in this mode, PAN502x is set in a power down mode and consumes very little power, which will help to prolong the standby time for the portable devices. PAN502 can only be waked up by “nRST” from host after entering into this mode.

2.3. Host Interface

The serial interface of PAN502x is I²C or SPI. PAN5020 supports I²C and SPI interfaces, and PAN5021 only supports I²C interface. The details of these interfaces are detailed in Section 2.4. The interrupt signal (INT) is used for PAN502x to inform the host to receive the ready data.

2.4. Serial Interface

2.4.1. I²C

The I²C can only be configured in the Slave mode. The data transfer format is shown in Figure 2-2. Figure 2-3 to Figure 2-8 show the various types of host read and write abstract data transfer format, including single write, random write, incremental write, single read, incremental read and spin on read. As for spin on read, it means that the host keeps reading an address until the read data hit the expected value.

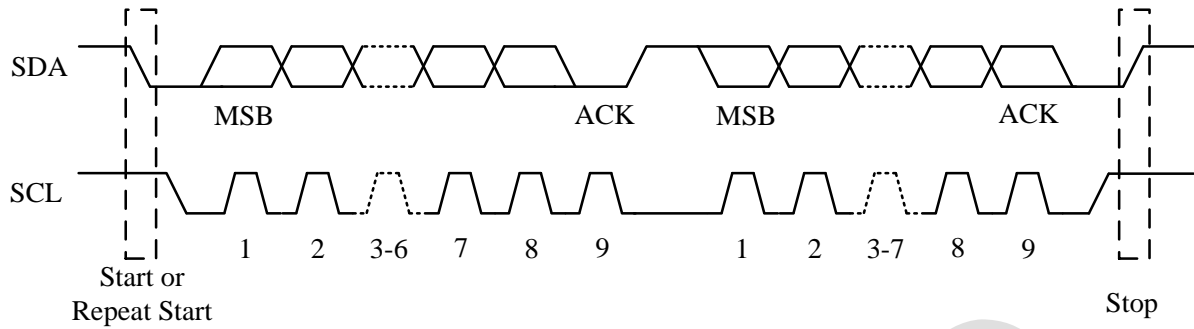


Figure 2-2 I2C data transfer format

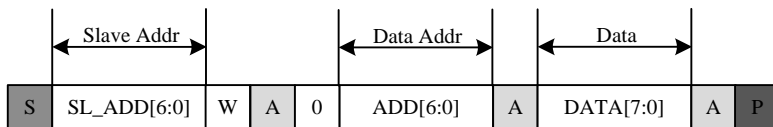


Figure 2-3 Single Write

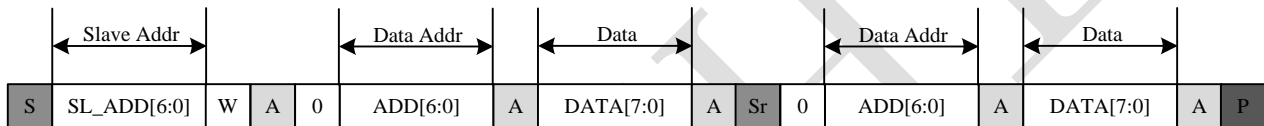


Figure 2-4 Random write

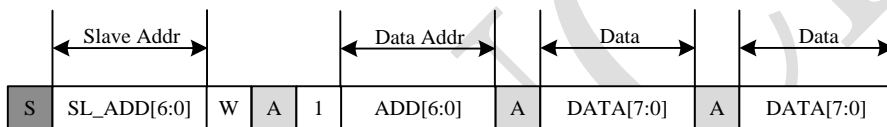


Figure 2-5 Incremental write

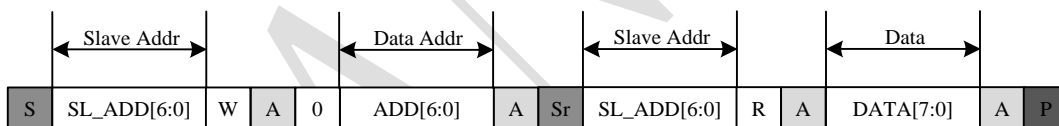


Figure 2-6 Signal read

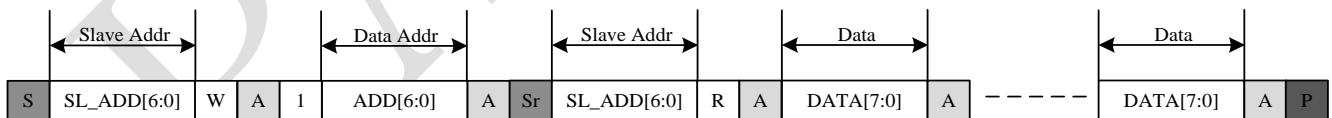


Figure 2-7 Incremental read

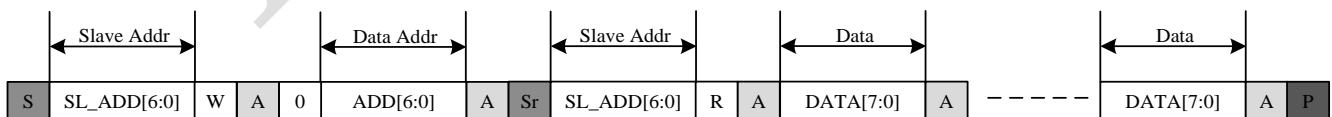


Figure 2-8 Spin on read

Table 2-1 lists the meanings of the mnemonics used in the above figures

Table 2-1 Mnemonics Description

Mmnemonics	Description
S	I2C Start or I2C Restart.
SL_ADD[6:0]	Slave address. AL_ADD[6:0]:address bits are identical to those of I2CADDR[7:1] register
R/W	'1' for read, '0' for write.
A(N)	ACK(NACK).
P	STOP: the indication of the end of a packet (if this bit is missing, S will indicate the end of the current packet and the beginning of the next packet).

2.4.2.SPI

SPI is a 4 wires serial interface. Like I2C, SPI can only be configured in salve mode as well. The following lists the 4 wires:

- SCK: serial data clock
- MOSI: data line from master to slave
- MISO: data line from slave to master
- NCS: active low select signal

Just like most widely used SPI data transfer format classification, it is always distinguished by clock polarity (CPOL) & clock phase (CPHA), therefore there are four kinds of data transfer formats. PAN502x supports one of these formats: CPOL=1 and CPHA=0. It means SCK is high when no data transportation, and slave device samples data at positive edge of SCK and sends data at negative edge of SCK. SPI transfers data at 8bit packets and the data transfer format is shown in Figure 2-9.

PAN502x supports the standard SPI host read and write modes, including single write, random write, single read, random read, and hybrid read and write, the abstract data transfer formats of these modes are shown in Figure 2-10 to Figure 2-14 respectively.

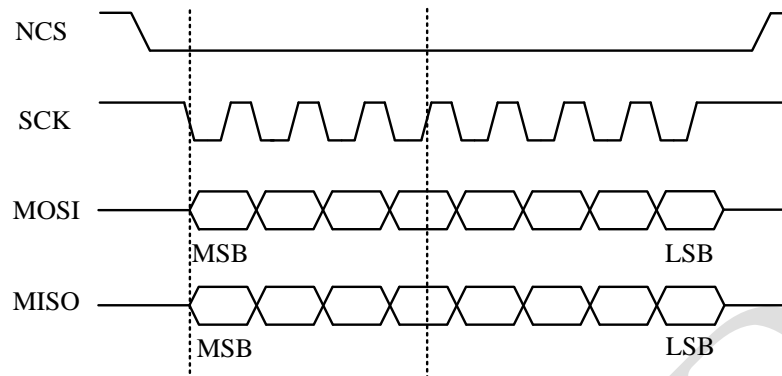


Figure 2-9 SPI Data Transfer Format

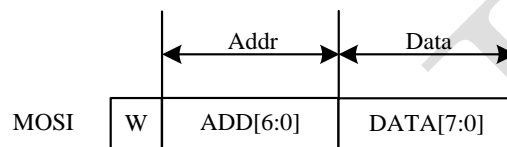


Figure 2-10 Single write

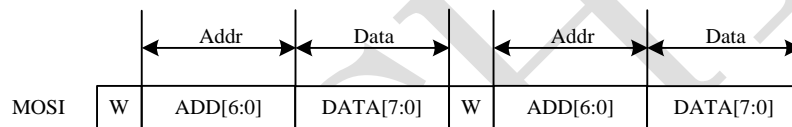


Figure 2-11 Random write

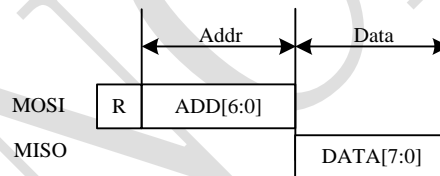


Figure 2-12 Signal read

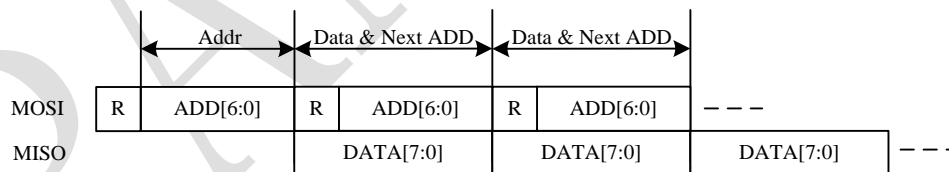


Figure 2-13 Random read

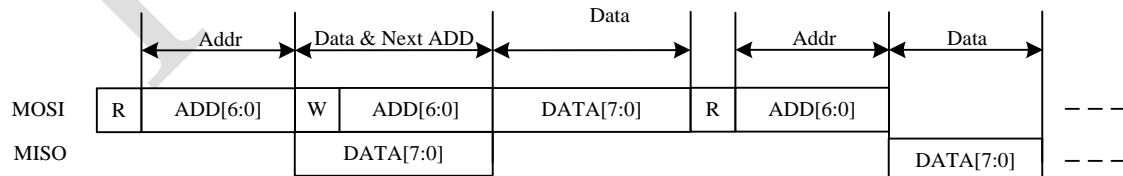


Figure 2-14 Hybrid read and write

3. Electrical Characteristics

Electrical characteristics over recommended operating conditions.

Typical values@25°C ,VDD3=3.3V, VDDA=3.3V, IO_VCC=1.8V, 48Pin QFN.

Table 3-1 DC Electrical Specification

Parameter		Min	Typ	Max	Units	Notes
VDD3=3.3V	Run	-	15	-	mA	Report Rate=150Hz No touch
VDDA=3.3V	Monitor	-	4.5	-	mA	Report Rate=30Hz No touch
With Internal Regulator	Shut down	-	35	-	μA	
IO_VCC=1.8V		-	1	-	μA	

Table 3-2 AC Electrical Specification

Parameter		Min	Typ	Max	Units	Notes
Power up delay		-	5	-	ms	
Reset		20	-	-	us	Active Low
Touch Report Rate		-	150	-	Hz	
Resume from shutdown		-	-	500	ms	Resume from shutdown to normal operation (navigation ready)
I ² C Interface Speed		-	400	-	kHz	
SPI Interface speed		-	10	-	MHz	

Table 3-3 Absolute Maximum Ratings

Parameter		Min	Type	Max	Units	Notes
Storage Temperature		-60	25	100	°C	
Operating Temperature		-20	25	85	°C	
Supply Voltage	With	VDD3				
Internal Regulator		VDDA	2.8	3	3.6	V
		IO_VCC	0	-	3.6	V

Notes:

1. There is no specific power supply turn-on or turn-off sequence requirement.
2. If the device experiences a supply-brown out condition (i.e. if either supply voltage goes below the minimum values specified), the contents of the registers can be corrupted. Therefore PAN502x suggests that the host hold nRST low at some time when all supply voltages have returned to their specified values, and then set nRST back to High for normal operation.

4. Pin Description

4.1 Pin Map

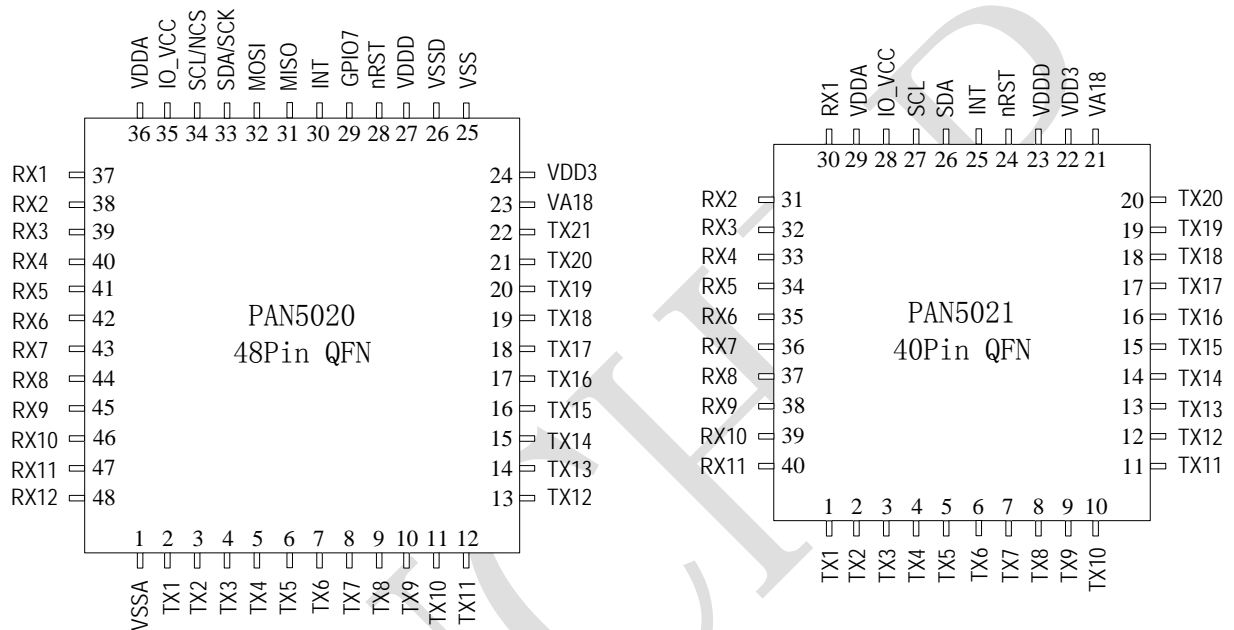


Figure 4-1 PAN502x Package Diagram

4.2 PAN502x Pin Description

Pin NO. PAN5020	Pin NO. PAN5021	Name	Type	
1		VSSA	PWR	Analog ground
2	1	TX1	O	Drive output
3	2	TX2	O	Drive output
4	3	TX3	O	Drive output
5	4	TX4	O	Drive output
6	5	TX5	O	Drive output
7	6	TX6	O	Drive output
8	7	TX7	O	Drive output
9	8	TX8	O	Drive output
10	9	TX9	O	Drive output
11	10	TX10	O	Drive output
12	11	TX11	O	Drive output

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13	12	TX12	O	Drive output
14	13	TX13	O	Drive output
15	14	TX14	O	Drive output
16	15	TX15	O	Drive output
17	16	TX16	O	Drive output
18	17	TX17	O	Drive output
19	18	TX18	O	Drive output
20	19	TX19	O	Drive output
21	20	TX20	O	Drive output
22		TX21	O	Drive output
23	21	VA18	PWR	internal generated 1.8V power supply, A 1 μ F ceramic capacitor to ground is required.
24	22	VDD3	PWR	PMU power supply,2.8V~3.6V
25		VSS	PWR	Analog ground
26		VSSD	PWR	Digital ground
27	23	VDDD	PWR	Digital power supply, generated internal. A 1 μ F ceramic capacitor to ground is required.
28	24	nRST	I	External Reset, active low
29		GPIO	I/O	General Purpose Input/Output port
30	25	INT	I/O	Interrupt request to the host
31		MISO	I/O	SPI Slave mode, data output
32		MOSI	I/O	SPI Slave mode, data input
33	26	SDA/SCK	I/O	I2C data input and output / SPI Slave mode, clock input
34	27	SCL/NCS	I/O	I2C clock input / SPI Slave mode, chip select, active low
35	28	IO_VCC	PWR	I/O power supply
36	29	VDDA	PWR	Analog power supply, 2.8V~3.6V.
37	30	RX1	I	Sense input
38	31	RX2	I	Sense input
39	32	RX3	I	Sense input
40	33	RX4	I	Sense input
41	34	RX5	I	Sense input
42	35	RX6	I	Sense input
43	36	RX7	I	Sense input
44	37	RX8	I	Sense input
45	38	RX9	I	Sense input
46	39	RX10	I	Sense input
47	40	RX11	I	Sense input
48		RX12	I	Sense input

5. Package

5.1. PAN5020 QFN-6x6-48L

Package Information of PAN5020 QFN-6x6-48L Package

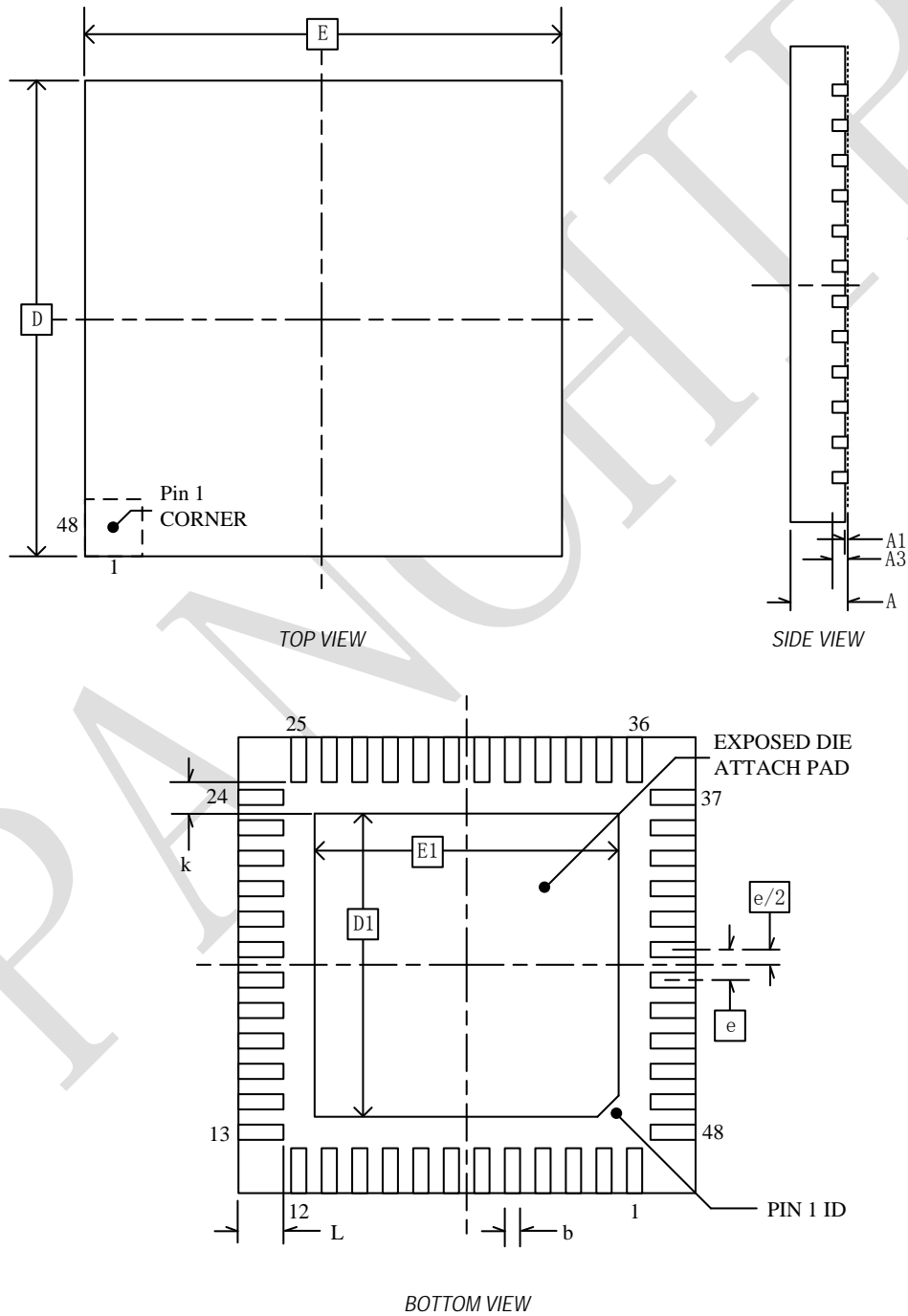


Figure 5-1 Top view, side view and bottom view of PAN5020

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Table 5-1 lists the meanings of the mnemonics used in Figure 5-1.

Table 5-1 Mnemonics description of PAN5020 package

Item	Symbol	Milimeter		
		Min	Typ	Max
Total Thickness	A	0.500	0.550	0.600
Stand Off	A1	0	0.025	0.05
L/F Thickness	A3	0.203 REF		
Lead Width	b	0.150	0.200	0.250
Body Size	D	5.924	6.000	6.076
	E	5.924	6.000	6.076
Lead Pitch	e	0.400 TYP		
EP Size	D1	3.700	3.800	3.900
	E1	3.700	3.800	3.900
Lead Length	L	0.324	0.400	0.476
	k	0.200 MIN		

5.2. PAN5021 QFN-5x5-40L

Package Information of PAN5021 QFN-5x5-40L Package

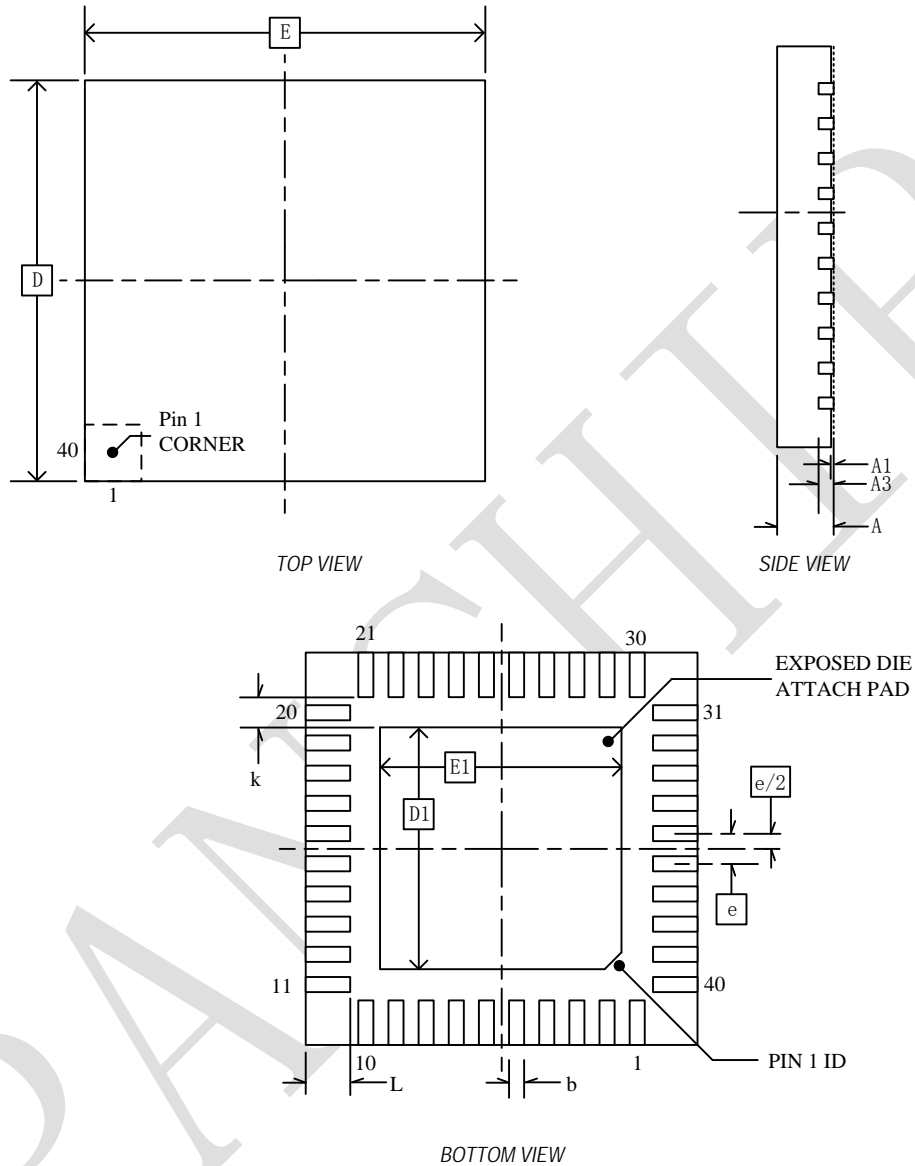


Figure 5-2 Top view, side view and bottom view of PAN5021

Table 5-2 lists the meanings of the mnemonics used in Figure 5-2.

Table 5-2 Mnemonics description of 40Pin package

Item	Symbol	Milimeter		
		Min	Typ	Max
Total Thickness	A	0.5	0.55	0.6
Stand Off	A1	0	0.025	0.05
L/F Thickness	A3	0.203 REF		
Lead Width	b	0.15	0.20	0.25
Body Size	D	4.924	5.000	5.076
	E	4.924	5.000	5.076
Lead Pitch	e	0.400 TYP		
EP Size	D1	3.500	3.600	3.700
	E1	3.500	3.600	3.700
Lead Length	L	0.324	0.400	0.476
	k	0.200 MIN		

6. Revision History

Version	Date	Description
V1.0	2014-03-03	Initial version

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